Integral University, Lucknow

Effective from Session:							
Course Code	**EC501**	**Title of the Course**	**Semiconductor Device Modeling & Circuit Simulation**	**L**	**T**	**P**	**C**
Year	**I**	**Semester**	I	**3**	**1**	**0**	**4**
Pre-Requisite	VLSI Design	**Co-requisite**					
Course Objectives	1. To introduce the operating principles of electronic circuits. 2. Several classes of semiconductor devices will be covered in this subject. 3. Semiconductor devices, BJT and its second order effects, FET and its second order effects . 4. An introduction to different circuits simulation will also be given.						

Course Outcomes	
CO1	Student will be able to understand the Compound semiconductors
CO2	Students will be able to understand and analyze the basics of semiconductor devices and their second order effects
CO3	For a given Model, Students will be able to understand about the models, analyze and examine the various models
CO4	Students will be able to understand second order effects of second order effects
CO5	Students will be able to understand various types of circuits models for MOSFET

Unit No.	Title of the Unit	Content of Unit	Contact Hrs.	Mapped CO
1	Compound semiconductors	Compound semiconductors, Lattice structures, Carrier drift, Direct and indirect semiconductors Scattering, Recombination, Mean life time, Continuity equation	8	1
2	PN junction, BJT characteristics	PN junction characteristics, Current components in diode, Equivalent circuits of diode, BJT characteristics, Second order effects in BJT: Thermal runaway, Base width modulation, Kirk effect, Band gap narrowing, Small signal analysis.	8	2
3	Models	Eber's moll model, Hybrid pi model, Figure of merit, approximate model and complete equivalent model of BJT, Charge control model, Gummel poon model, SPICE model of BJT, Simulation of BJT	8	3
4	Second Order Effects of MOS	N-channel, P-channel MOS characteristics and features, Enhancement and depletion mode: second order effects of MOS: Body effect, Channel length modulation, Subthreshold conduction, DIBL, Hot carrier effect, Mobility degradation, Velocity saturation, CMOS latch up, MOS parasitic capacitances and resistances.	8	4
5	Circuits models for MOSFET	Circuits models for MOSFET: small signal, SPICE models, BSIM model, Simulation and Layout design DC, AC and Transient analysis of linear and nonlinear circuits, logic and timing simulations.	8	5

Reference Books:

1. Baker, Li, Boyce "CMOS Layout, Design and simulation", PHI 4. Sze S.M. " Semiconductor Physics" MacGraw Hill publication
2. Rabaey Jan M, Chandrakasan Anantha, Nikolic Borivoje "Digital Integrated Circuits" PHI publication
3. Kanno Kannan " Semiconductor Devices and Physics" Wiley publication
4. Millman, Halkias " Electronic Devices and Circuits" TMH publication

e-Learning Source:

5. https://onlinecourses.nptel.ac.in/noc21_ee80/preview
6. https://digimat.in/nptel/courses/video/117106033/L35.html

	Course Articulation Matrix: (Mapping of COs with POs and PSOs)																	
PO-PSO CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	PSO4	PSO5	PSO6
CO1	**3**	**2**										**2**	1					
CO2	**3**	**2**											2		2			
CO3	**3**	**2**	**3**										1	2		2		

CO4	**3**	**3**	**3**	**3**										1	1	3		
CO5	**3**					**3**		**1**				**2**	2	2	1			

1- Low Correlation; 2- Moderate Correlation; 3- Substantial Correlation

Name & Sign of Program Coordinator	**Sign & Seal of HoD**

Integral University, Lucknow

Effective from Session:							
Course Code	EC502	**Title of the Course**	VLSI Devices & Circuits	**L**	**T**	**P**	**C**
Year	I	**Semester**	I	**3**	**1**	**0**	**4**
Pre-Requisite	SC Devices and IC Technology	**Co-requisite**					
Course Objectives	• To understand the underlying concepts and VLSI Perspectives. • To learn the analysis of a MOS circuits and systems and encoding of VLSI systems for fabrication. • To learn how the parasites arise and affect the circuits and systems performance. Simple speed improvement techniques. • To learn the design methodologies and simulation of the MOS based circuits.						

Course Outcomes	
CO1	Given a system Students shall be able to understand properties of digital systems, regenerative property, NMOS, PMOS, pull up and pull-down networks, NAND/NOR, EX-OR, Decoder and short channel effects.
CO2	For a given system, student shall be able to analyze standard CMOS circuits, Pseudo NMOS, Pass Transistor Logic (PTL), Transmission gate Adder/ Subtractor, Design of Combinational circuits and Sizing of MOSFETs.
CO3	For a given Sequential Circuit system students can understand Latches & Flip-flops and Dynamic CMOS and Domino CMOS.
CO4	Students shall be able to identify the technology for Standard cells, Circuit implementation using PAL and PLA, FPGA, Look up tables (LUTs).
CO5	For a given a system, able to design RAM, ROM, basic cells of SRAM and DRAM, GaAs MESFET and Bi-CMOS: features, inverter, conventional and full swing BiCMOS circuits.

Unit No.	Title of the Unit	Content of Unit	Contact Hrs.	Mapped CO
1	Digital System	Properties of digital systems, regenerative property, NMOS, PMOS, pull up and pull-down networks, strong 1 and strong 0, NAND/NOR, EX-OR, Decoder, MUX, Micron and Sub-micron devices: Scaling, Short channel effects	8	1
2	CMOS Circuits	Standard CMOS circuits, Pseudo NMOS, Pass Transistor Logic (PTL), types of PTL, advantages and disadvantages of PTL, Level restorer, Transmission gate Adder/ Subtractor, Design of Combinational circuits and Sizing of MOSFETs	8	2
3	Sequential Circuits	Dynamic CMOS and Domino CMOS, Complex gates, Sequential Circuits: Latches & Flip-flops, Problems of race, race around and 1's catching	8	3
4	PLDs	Standard cells, Circuit implementation using PAL and PLA, FPGA, Look up tables (LUTs), Importance of FPGA	8	4
5	Memories	RAM, ROM, basic cells of SRAM and DRAM, 6T RAM, 3T RAM, 1T RAM, GaAs MESFET, its characteristics and applications, Bi-CMOS: features, inverter, conventional and full swing BiCMOS circuits.	8	5

Reference Books:

- Rabaey Jan M, Chandrakasan Anantha, Nikolic Borivoje " Digital Integrated Circuits" PHI publication.
- Hodges, Jackson, Saleh "Analysis and Design of Digital Integrated Circuits" McGraw Hill publication.
- Kang Sung-Mo, Leblebici Yusuf "CMOS Digital Integrated Circuits" Tata McGraw Hill publication.
- Rabaey Jan M, Chandrakasan Anantha, Nikolic Borivoje " Digital Integrated Circuits" PHI publication.
- Hodges, Jackson, Saleh "Analysis and Design of Digital Integrated Circuits" McGraw Hill publication.
- Sedra ,Smith " Microelectronic Circuits" Oxford Publication
- Islam S.S "Semiconductor Devices and Physics" Oxford Publication

e-Learning Source:

https://www.slideshare.net/imrankhan2142/unit-1-traditional-cmos-design?qid=0a8c9b4a-990a-49e0-b30b-b6f7a41704d1&v=&b=&from_search=11

	Course Articulation Matrix: (Mapping of COs with POs and PSOs)															
PO-PSO CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	PSO4
CO1	3	2		2	1	1		1	2				3	2	1	1
CO2	3	2	1	2	1	1			2		1		3	2	1	1
CO3	3	3		1	2				1			1	3	2	2	1
CO4	3	1	2	3	2	1			1				2	1	2	1
CO5	3	3	2	2	1	1			1				2	1	2	1

1- Low Correlation; 2- Moderate Correlation; 3- Substantial Correlation

Name & Sign of Program Coordinator	**Sign & Seal of HoD**

Integral University, Lucknow

Effective from Session:							
Course Code	EC503	**Title of the Course**	Microelectronics Technology	**L**	**T**	**P**	**C**
Year	I	**Semester**	I	**3**	**1**	**0**	**4**
Pre-Requisite	Electronic Devices and Circuits (EC-201)	**Co-requisite**					
Course Objectives	• Introduction to different types of integrated circuits. To learn about the silicon wafer preparation techniques, cleaning of wafers, crystal orientation and different epitaxial process. • To understand different types of oxidation techniques, thickness measurement of oxide and different oxide furnaces. To understand the dopant diffusion processes its models and different diffusion furnaces. • To learn about different photolithography and mask making and pattern transfer process. • To learn about different ion implantation techniques, its equipment, range and dopant distribution profiles. Introduction of chemical vapor deposition (CVD) and CVD process in IC fabrication. • To study about different fabrication steps of IC such as bipolar IC, MOS IC, and BiCMOS IC technology. To know about fault modeling, and characterization technique.						

Course Outcomes	
CO1	Students will be able to identify basic structure of BJT, NMOS, CMOS, BiCMOS Devices. Students will know about Crystal Growth & Silicon wafer preparation, cleaning and crystal orientation and defects. Students will able to compute different vapor phase epitaxial process and redistribution of impurities during epitaxy.
CO2	Students shall able to understand different types of oxidation techniques and different oxide furnaces. Students will able to compute the thickness of the oxide. Students will able to understand dielectrics and polysilicon film deposition.
CO3	Student shall be able to select the suitable photolithography. To make mask making learn about pattern transfer process.
CO4	Students will able to understand identify different ion implantation equipment and its process. Students will able to compute range and dopant distribution profiles. Develop an understanding about chemical vapor deposition (CVD) and CVD process in IC fabrication.
CO5	Student shall be able to explain about fabrication steps of IC such as bipolar IC, MOS IC, and BiCMOS IC technology. To know about fault detection and characterization technique.

Unit No.	Title of the Unit	Content of Unit	Contact Hrs.	Mapped CO
1	Introduction, Crystal Growth & Silicon wafer preparation and Epitaxy	• Basic structure of BJT, NMOS, CMOS, BiCMOS Devices. • Introduction, Structure of Semiconductor, Electron- Grade Silicon, CZ Crystal Growth, Silicon Shaping, Processing considerations. • Introduction, Vapour-Phase Epitaxy, Molecular beam Epitaxy, Silicon on Insulator, Epitaxial Evaluation.	8	1
2	Oxidation & Dielectrics and Polysilicon Film Deposition	• Introduction, Growth Mechanism and Kinetics, Thin oxidation, Oxidation Technique and System, Oxidation Properties, Redistribution of Dopants at interface, Oxidation of Polysilicon, Oxidation Induced Defects. • Introduction, Deposition Process, polysilicon, Silicon Dioxide, Silicon Nitride, Plasma Assisted Deposition.	8	2
3	Lithography, Etching & Diffusion	• Introduction, Optical Lithography, Electron Lithography, X-ray Lithography, Ion Lithography. • Wet and Dry Chemical Etching, Reactive Plasma Etching. • Introduction, Model of diffusion, in solid, Diffusivities of B, P, As and Sb, Measurement Techniques.	8	3
4	Ion Implantation & Metallization	• Introduction, Range Theory (Jon Stopping, Range Distribution, Damages, Channeling), Annealing, Shallow Junction, High Energy Implantation. • Chemical Vapour Deposition (CVD), Physical Vapour Deposition (PVD), Evaporation technique, sputtering technique.	8	4
5	Fabrication steps of IC	• Bipolar IC, MOS IC, BiCMOS IC, Fault Detection and Characterization Technique.	8	5

Reference Books:

- SZE S M (SE) "VLSI Technology", Mc Graw Hill International.
- Gandhi S, "VLSI fabrication principles", Wiley Publication.

- Campbell S A, “The Science and Engineering of Microelectronics fabrication” Oxford University press.
- Geiger Randall L, Allen Phillip E, Stader Noel R, “VLSI Design Technique for Analog and Digital Circuits”, Mc Graw Hill International.

e-Learning Source:

https://onlinecourses.nptel.ac.in/noc21_ee86/preview

https://youtu.be/366BVdmcUxk

	Course Articulation Matrix: (Mapping of COs with POs and PSOs)															
PO-PSO CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	PSO4
CO1	3	3	1	2	1	1		1	2				3	2	1	1
CO2	3	1		3	2	1			2		1		3	2	1	1
CO3	3	3		1	2	1			1			1	3	2	2	1
CO4	3	1	2	3	2	1			1				2	1	2	1
CO5	3	3	2	2	1	1			1				2	1	2	1

1- Low Correlation; 2- Moderate Correlation; 3- Substantial Correlation

Name & Sign of Program Coordinator	**Sign & Seal of HoD**

Integral University, Lucknow

Effective from Session:							
Course Code	**EC504**	**Title of the Course**	**Digital System Design using Verilog HDL**	**L**	**T**	**P**	**C**
Year	**1**	**Semester**	1	3	1	0	4
Pre-Requisite	NA	**Co-requisite**	NA				
Course Objectives	• Improve the student's background and basic knowledge in the fields of HDL programming. • Improve the student's skills in the logical design of digital systems. • To explain combinational ,sequential circuits and Concept of PLA and PLDs. • To explain the verilog HDL with detailed study of structural data flow and behavioral modeling. •To explain the test bench and simulation of combinational and sequential circuits • To Study of RTL Coding Guidelines, Modelsim Simulation Tool, Synthesis Tool, Synplify Tool, Xilinx Place & Route Tool. • Design of Memories – ROM, RAM , Design of Arithmetic Circuits, System Design						

Course Outcomes	
CO1	Student will be able to understand the concept of VLSI Design flow and will able design the combinational circuit using PLDs and PAL.
CO2	Student will able design the sequential circuit i.e. different types of registers and counters etc. Student will be able to understand the concept of Design Flow of VLSI Circuits
CO3	Student will be able to explain HDL languages and its type .Student will able to design combinational and sequential circuit using structural modeling, dataflow modeling and behavioral modeling of Verilog HDL
CO4	Student will able to write the test bench of digital circuits. Student will able to design system using ASM Chart , able to work on Modelsim and will able to simulate the combinational and sequential circuit on it.
CO5	Student will able to design the ROM , RAM , arithmetic circuits and system like ATM machine , weighing machine etc. using Verilog HDL.

Unit No.	**Title of the Unit**	**Content of Unit**	**Contact Hrs.**	**Mapped CO**
1		Introduction to VLSI Design, Combinational Circuit Design, Programmable Logic Devices, Programmable Array Logic.	8	1
2		Review of Flip-Flops, Sequential Circuits, Sequential Circuit Design, Design Flow of VLSI Circuits.	8	2
3		Verilog Modeling of Combinational Circuits, Modeling of Verilog Sequential Circuits, RTL Coding Guidelines, Coding Organization - Complete Realization.	8	3
4		Writing a Test Bench, System Design using ASM Chart, Example of System Design using ASM Chart, Examples of System Design using Sequential Circuits, Simulation of Combinational and Sequential Circuits, Analysis of Waveforms using Modelsim.	8	4
5		Model Sim Simulation Tool, Synthesis Tool, Synplify Tool - Schematic Circuit Diagram View, Xilinx Place & Route Tool, Design of Memories – ROM, RAM , Design of Arithmetic Circuits, System Design Examples.	8	5

Reference Books:

1. "John F Wakerley,"Digital Design Principles and Practice", PHI

2. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", PHI.

e-Learning Source:

	Course Articulation Matrix: (Mapping of COs with POs and PSOs)																	
PO-PSO CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO4	PSO5	PSO6	PSO7
CO1	**3**	**3**	**3**	**1**					**2**		**1**	**3**	**3**	**3**				
CO2	**3**	**3**	**3**	**1**					**2**		**2**	**3**	**2**	**3**				
CO3	**3**	**3**	**3**	**3**	**3**		**2**	**2**	**2**		**2**	**3**	**3**	**3**				
CO4	**3**	**3**	**3**	**3**	**3**		**2**	**2**	**2**	**2**	**2**	**3**	**3**	**3**				
CO5	**3**	**3**	**3**	**3**	**3**	**1**	**3**	**3**	**2**	**2**	**2**	**3**	**1**	**1**				

1- Low Correlation; 2- Moderate Correlation; 3- Substantial Correlation

Name & Sign of Program Coordinator	**Sign & Seal of HoD**

Integral University, Lucknow

Effective from Session: 2022-23							
Course Code	EC505	**Title of the Course**	Device Modeling & Circuits Simulation Lab	**L**	**T**	**P**	**C**
Year	I	**Semester**	I	**0**	**0**	**2**	**1**
Pre-Requisite	EC505	**Co-requisite**					
Course Objectives	• To understand basic experimental technique to determine impact of NMOS inverter and micron technology. • To learn basic experimental technique to determine • To understand basic experimental technique to determine efficiency of positive displacement pump i.e. Reciprocating • pump and Gear oil pump. • Demonstrate basic experimental technique to determine efficiency of hydraulic ram.						

Course Outcomes	
CO1	Demonstrate basic experimental technique to determine impact of NMOS inverter.
CO2	Demonstrate basic experimental technique to determine symmetrical & delay CMOS inverter.
CO3	Demonstrate basic experimental technique to two input CMOS NAND Inverter. pump and Gear oil pump.
CO4	Design current mirror for given basic component.
CO5	Determine and design power consumption CMOS and CMOS SCHMITT trigger.

Experiment No.	**Title of the Experiment**	**Content of Unit**	**Contact Hrs.**	**Mapped CO**
1	NMOS INVERTER	Design a depletion load NMOS inverter VOL <= 0.3 in 5 micron technology V_{TOD} 1volt V_{TOL}=3volt kpl=40 micron amp/volt^{2}kpd 10 micron amp/volt^2 VDD=5 volt. For the above data simulate vtc for lambda 0.05 gamma 0.4 v also calculate noise margin and inverter threshold Voltage.	2	CO1
2	SYMMETRICAL CMOS INVERTER	Design a symmetrical CMOS inverter for a given data VDD=5 volt VTP=VTN=1volt for 5 micron technology kpl=40 micron amp/volt^{2}kpd 10 micron amp/volt^2 for lambda 0.05 gamma 0.4 v calculate (I) VM for VTC (II) calculate noise margin (III) What is minimum CMOS inverter size (IV) Plot VTC with and without body effect Design a parallel CMOS Inverter.	2	CO1
3	DELAY CMOS INVERTER	Design a CMOS inverter delay not more than 100ps for any transition assume 5 micron technology VTN=0.9 V and VTP=1.1 V, VDD=5V,CL=10 PF, Kn=8 micron, MPL per Volt^2	2	CO2
4	TWO I/P CMOS NAND INVERTER	Design a two i/p CMOS NAND inverter plots it's VTC and verified its truth table	2	CO2
5	TWO I/P CMOS NOR INVERTER	Design a two i/p CMOS NOR inverter plots its VTC and verified its truth table.	2	CO3
6	CURRENT MIRROR	Design a current mirror using 5 micron technology to supply 5micron amp load current KP=12Micron,Kn=30micron,VTP=-1.1,VTN=0.9, lambda 0.05 gamma 0.4 v. Plot o/p current and maximum load resistant	2	CO3
7	POWER CONSUMPTION CMOS	Determine the power consumption by CMOS inverter completing one switching operation with help of power VDD=5V, CL=1pf, CY=100pf RY=100K determine the effect of lamda on power study the power reported by SPICE in o/p file.	2	CO4
8	CMOS SCHMITT TRIGGER	Design a CMOS Schmitt trigger circuit with two different threshold voltage for increasing and decreasing input signal. Plot the simulated VTC for CMOS Schmitt trigger also determine threshold voltage for low to high and high to low switching event in noisy environment for the following parameters VTN=1V, VTP=-1V, VDD=5V, KP=2.5e^{-5}	2	CO5
e-Learning Source:				

https://www.vlab.co.in/

	Course Articulation Matrix: (Mapping of COs with POs and PSOs)														
PO-PSO CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3	2	3	2	3		1	3	2		3	3	2	2
CO2	3	2	1		1		1					3	2	1	1
CO3	3	1	1	1	1							3	2	1	
CO4	3	2			1	1						3	2	1	1
CO5	3	1			1							3	2	1	

1- Low Correlation; 2- Moderate Correlation; 3- Substantial Correlation

Name & Sign of Program Coordinator	**Sign & Seal of HoD**